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METHOD FOR FORMING FIELD OXIDE FILM
[Fiirudo sanka maku no keisei hoho]

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Specifications /1[*]

1. Title of Invention

Method for Forming Field Oxide Film

2. Claim(s)

1. A method for forming a field oxide film for a semiconductor device comprising the steps of: successively forming an oxide film and a nitride film on a silicon semiconductor substrate; removing some of said nitride film in the upper region of the part which will be the field region of the substrate to expose said oxide film, and at the same time, leaving said remainder of nitride film behind as a mask for selective oxidation; subjecting the central portion of the above-mentioned field region of the substrate to ion implantation with any of Si, O or Ar ions through the above-mentioned exposed oxide film to form an implantation defect in said central portion; and selectively oxidizing the substrate field region by using the above-mentioned oxide film mask to form a field oxide film with a deep shape in said central portion, and at the same time, gettering lattice defects generated in the proximity of the circumference of said field oxide film into the above-mentioned implantation defect.

3. Detailed Specifications

[Technical Field of the Invention]

The present invention relates to a method for forming a field oxide film for a semiconductor device, and specifically it relates to

[*] Numbers in the margin indicate pagination in the foreign text.

a method for selectively oxidizing a field oxide film improved by adding a pretreatment step in which a gettering defect region is formed prior to the oxidation.

[Technical Background of the Invention]

A method for forming a field oxide film in a selective oxidation (LOCOS) method has been performed in the past. This will be described with reference to the process drawings in Figures 2(a) to (d).

First of all, as in Figure 2(a), an approximately 100Å thick SiO_2 film 2 is formed on a silicon substrate 1 in a dry oxidation method, and then a 600 to 3,000Å thick Si_3N_4 film 3 is formed on this SiO_2 film 2 in a CVD (chemical vapor phase growth) method.

Next, a resist patterning for forming an opening corresponding to the field region is performed on the Si_3N_4 film 3 in a lithography technique, and as in Figure 2(b), the Si_3N_4 film and SiO_2 film in the upper part of the field region are etched off, leaving behind a /2
mask comprising an Si_3N_4 film 3a and SiO_2 film 2a for selective oxidation, and then a field patterning is performed.

And after that, as in Figure 2(c), using the remaining Si_3N_4 film 3a and SiO_2 film 2a, a 1 μm or thicker field oxide film is formed in the field region of the substrate by wet oxidation.

And finally, as in Figure 2(d), the masks 3a and 2a are removed to complete element isolation. After removing the masks, element formation is performed on the substrate part, and a semiconductor device is constructed.

[Problems of the Background Art]

In the aforesaid conventional selective oxidation method, due to the difference in the coefficient of thermal expansion between the silicon substrate and the field oxide film (SiO_2 film), heat stress is generated especially in the circumferential interface (pattern edge) of the field oxide film. Because the breakdown voltage of the field oxide film increases, and so forth, if the interfacial stress thereof is extremely large, cracking of the insulation film is caused, an abnormality phenomenon at the pattern edge is evoked during impurity diffusion, or an anomaly is brought out during electrode formation or etching.

In addition, a difference in the coefficient of thermal expansion between the silicon substrate and field oxide film causes irregularities in the substrate, and as a result, because defects in and transfer to the substrate occur, the reliability of the element diminished, and in particular, degradation due to the irregularities owing to the heat cycle and the like causes an increase in the leak current at a junction and a leak current at the pattern edge, which are the primary causes of a decrease in yield.

[Purpose of the Invention]

An object of the present invention is to provide a method for forming a field oxide film which can reduce a leak current by increasing the breakdown voltage of an insulation film by forming a thick oxide film, and at the same time, gettering the defects at the

pattern edge into defect regions generated in the ion implantation part by subjecting the central part of the field region to an ion implantation as a pretreatment step for field oxidation.

[Outline of the Invention]

The present invention was accomplished to achieve the above-mentioned object. That is, the Si_3N_4 in the upper region of the field region of the substrate is removed to expose the SiO_2 film there, after which only the central portion of the substrate field region is opened in the surface of the exposed SiO_2 film, a resist pattern enabling ion implantation is formed by a lithography technique, and then ion implantation of either Si, O or Ar is performed by using this resist pattern as the mask, and an implantation defect part is formed in the part of the central portion of the field region with the prescribed depth. Due to the selective oxidation step, lattice defects generated in particular at the pattern edge of the field oxide film were gettered into the implantation defect part, and at the same time, selective oxidation proceeded in this central portion, and a field oxide film having a shape concealed deeply in the substrate was formed, whereby element isolation characteristics having little leak current at a high breakdown voltage were possible.

[Practical Examples of the Invention]

A practical example of the method of the present invention will now be specifically described with reference to the process drawings

in Figures 1(a) to (d). Each drawing in Figure 1 depicted element cross sections.

First of all, as in Figure 1(a), a 500Å thick SiO_2 film 2 is formed on the silicon substrate 1 in a dry oxidation method, and further, a 1,000Å thick Si_3N_4 film 3 is formed on the SiO_2 film 2 in a CVD method. This step is the same as in the conventional selective oxidation method.

Next, this is masked by resist patterning (not shown), and only the Si_3N_4 film in the upper region of the substrate field region is removed by plasma etching to expose the SiO_2 film 2a on the field region, as in Figure 1(b). In this case, the SiO_2 film 2 is left behind on the field region to obtain a protective film which prevents contamination of the substrate, which is different from a conventional method.

And then, in Figure 1(b), a central portion 2b is left behind on the field region of the exposed SiO_2 film 2 and a photoresist (KTFR) implantation mask 4 is formed on the entire substrate. The central portion of the field region of the silicon substrate is subjected to an ion implantation 5 of Si ions using the implantation mask 4 at an acceleration voltage of 180 keV and density of $2\times10^{15}/cm^2$. The ion implanted 5 Si ions pass through the SiO_2 film 2b and an implantation defect 6 is formed where the silicon substrate 1 is 1,000Å deep. /3

Subsequently, as shown in Figure 1(c), the implantation mask 4 is peeled, and by using the mask 3a of the Si_3N_4 film, a 1,100°C, 2-

hour wet oxidation is performed to form a 1.2 μm thick field oxide film 7. The central portion of the field region subjected to the ion implantation 5 oxidation proceeds to a 0.5 μm depth, and a field oxide film 7 is formed with a deeper shape only in this central portion 7a, which is different than in the conventional field oxide film. In addition, in this oxidation step, the implantation defect 6 is destroyed, coalesced or condensed repeatedly to getter the lattice defects at the pattern edge of the field oxide film.

Finally, as in Figure 1(d), the Si_3N_4 film 3a masked by selective oxidation is removed and the field oxide film 7 is completed.

[Advantages of the Invention]

According to the method for forming a field oxide film of the present invention, first of all, a semiconductor device in which a leak current is reduced at the pattern edge of the field oxide film is obtained. After the field oxide film in Figure 1(d) was completed and the Si_3N_4 film removed, an n^+ layer was formed in the p-type element formation region, the leak current value of the n^+-p junction was measured to find the frequency (Figure 3(a)), and meanwhile, the field oxide film of the conventional step was compared with the same measurement (Figure 3(b)).

The frequency of the method of the present invention in Figure 3(a) and the frequency of the conventional method in Figure 3(b) are compared, and as understood, it is seen that the leak current in method of the present invention is substantially one-third that in

the conventional method. This is a resulting phenomenon of the lattice defects at the pattern edge, which is the primary cause of the generation of a leak current, being reduced by gettering.

According to the method of the present invention, second of all, upon trying to measure the isolation breakdown voltage between junctions, according to the method of the present invention, it is 35 V, but it is 23 V according to the conventional method, and it is seen that excellent insulation and isolation characteristics are realized. The field oxide film having a high breakdown voltage obtained as such means that the degree of freedom for element isolation design is enhanced.

4. Brief Description of the Drawings

Figures 1(a) to (d) are element cross-sectional process drawings for explaining the steps of the method for forming a field oxide film of the present invention; Figures 2(a) to (d) are element cross-sectional process drawings depicting the steps of a conventional method for forming a field oxide film; and Figures 3(a) and (b) are graphs for explaining the advantages of the method of the present invention.

1: silicon substrate; 2: oxide film; 3: nitride film; 3a: nitride film mask (for selective oxidation); 4: implantation mask; 5: ion implantation; 6: implantation defect; 7: field oxide film; 7a: central portion of field oxide film

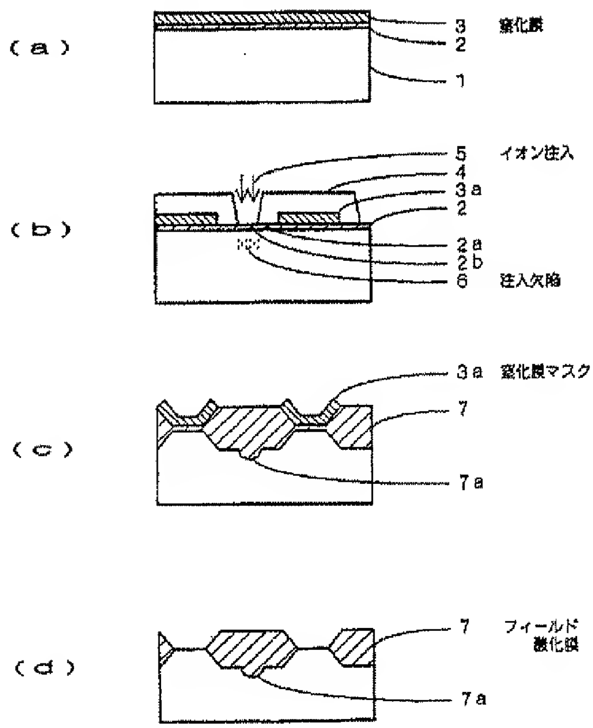


Figure 1

Key: 3: nitride film; 5: ion implantation; 6: implantation defect; 3a: nitride film mask; 7: field oxide film

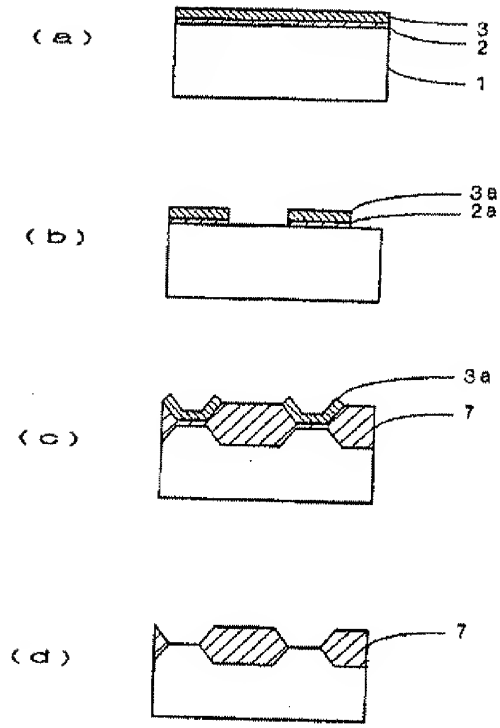
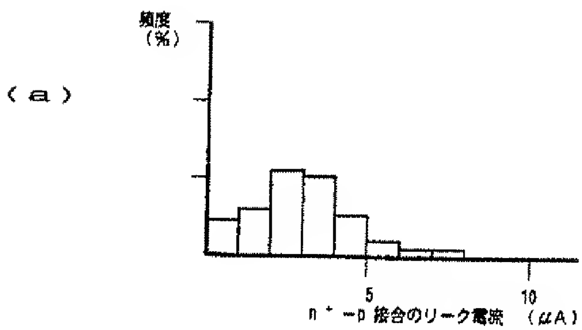
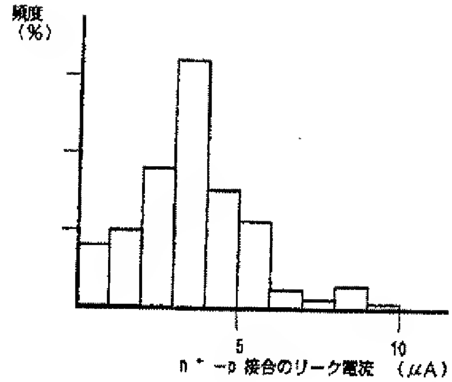


Figure 2



Key: (X-axis) n^+-p Junction Leak Current (μA); (Y-axis) Frequency (%)

(b)



Key: (X-axis) n^+-p Junction Leak Current (μA); (Y-axis) Frequency (%)

Figure 3